

J. . N. PAGE 1 OF 2 **GROUP ART** ATTACHMENT SERIAL NO. U.S. DEPARTMENT OF COMMERCE FORM PTO-892 TO PAPER NO. UNIT 6 PATENT AND TRADEMARK OFFICE 09/321,611 2133 APPLICANT(S) NOTICE OF REFERENCES CITED QU, DONGHUI **U.S. PATENT DOCUMENTS** FILING DATE SUB-CLASS CLASS NAME DATE DOCUMENT NO. 30 380 Matsuzaki et al. 3/1993 Α 5,199,070 708 650 Chung 9/2000 В 6,125,380 107 359 Boffi 8/2001 С 6,275,311 D Ε F G Н ı J Κ FOREIGN PATENT DOCUMENTS SUB-CLASS **CLASS** NAME COUNTRY DATE DOCUMENT NO. Μ Ν 0 Р Q OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.) Orton et al. (New fault tolerant techniques for residue number systems; IEEE, page(s): 1453 - 1464; Nov. R 1992) Stout (Basic Electrical Measurements; 2d Ed., 1960; pages 82-85.) Burgess (Efficient RNS to binary conversion using high-radix SRT division; IEEE; page(s): 1240 - 1243; 1-4 T Nov. 1998) Gala et al. (A high speed VLSI algorithm for A*B modulo N; IEEE, page(s): 389 - 392 vol.1; 12-14 Aug. 1990) U DATE EXAMINER September 28, 2001 GUY J. LAMARRE, P.E. Form892ccs2106b

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OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)									
	R	Bini et al. (Improved parallel polynomial division and its extensions; IEEE, page(s): 131 - 136; 24-27 Oct. 1992							
	s	Saha, A et al. (Design and FPGA implementation of efficient integer arithmetic algorithms; IEEE, page(s): 4 p; 4-7 April 1993)							
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GUY J. LAMARRE, P.E. September 28, 2001									

* A copy of this reference is not being furnished with this office action. (See Manual of Patent Examining Procedure, section 707.05(a).)